Architectures of a digital modulator for high-speed data transmission in telecommunication system

Architectures d'un modulateur numérique pour la transmission des données à haut débit dans le système de télécommunication

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ABSTRACT

Digital systems are more than necessary in our daily life. This last decade, the world is dealing with a remarkable technological revolution, especially, in the field of miniaturization of electronic devices such as modems and embedded systems. This work is focused on challenges of developing Quadrature amplitude modulation (QAM) digital modulators. In this context, this paper proposes several methods, simpler and efficient compared to the existing methods. The obtained results indicate that the proposed technique is effective in terms of data rotation calculation, particularly, for the sinusoidal signal generation in the QAM digital modulators. Through this study, an FPGA-based system with a maximum frequency of 550MHz is developed. The objective is to identify the optimal configuration facilitating data transmission in radio software. The obtained results were compared to recent works, and have showed a significant improvement in terms of computation time, especially in case of increasing the frequency of the transmission system at a very high rate.

RESUME

Les systèmes numériques sont de plus en plus nécessaires dans notre vie quotidienne. Cette dernière décennie, le monde traite une révolution technologique remarquable, en particulier, dans le domaine de la miniaturisation des appareils électroniques tels que les modems et les systèmes embarqués. Dans cette recherche, nous nous concentrons sur les défis des modulateurs numériques se développant de la modulation d'amplitude de quadrature (QAM). Dans ce contexte, cet article propose plusieurs méthodes, plus simples que celles existantes. Les résultats obtenus indiquent que notre proposition est efficace en termes de calcul de la rotation des données, en particulier pour la génération de signaux sinusoïdaux dans les modulateurs numériques QAM. Grâce à cette étude, nous avons développé un système basé sur FPGA avec une fréquence maximale de 550 MHz. Les résultats obtenus ont été comparés à des travaux récents, et ont montré une amélioration significative en termes de temps de calcul, notamment en cas d'augmentation de la fréquence du système de transmission à un débit très élevé

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1. INTRODUCTION

In order to facilitate data transmission in complex digital QAM modulators, several techniques were used, such as the methods based on bandwidth or high frequency [1]. The implementation of a digital transmission system relies heavily on rapid progress in the field of signal processing, integrated circuits and FPGA platforms [2]. Thus, the use of integrated solutions becomes indispensable as the level of complexity of the systems increases and that the price agreed by the consumer decreases.

The complex digital QAM modulator consists of five principal components: three components, namely the encoder, the phase accumulator, and the sine generator, operating digitally. The remaining two components, including the analog-to-digital converter and low pass filter, operating in analog mode [3].

In this paper, we mainly used the three first elements that generate a complete digital QAM modulator. The purposed modulator includes the transmission of the short-term signal with a high throughput. The interpretation of the performance realized by QAM modulator has done with the ISE 12.2 [4].

Related work

In broadband telecommunication there have been several studies conducted on the data transmission. These studies extend various relevant parameters that can contribute to improve the system performance, especially in terms of maximum frequency, cell and throughput. Recently, Winzer et al. [5] studied the effectiveness of the long-haul optical network spectral. They used a 256 -QAM modulation for generating a wavelength-division-multiplexed (WDM) long-haul transmission, and coherent detection of 112-Gb/s polarization-division-multiplex, with a fiber length of 1022 km. The resulting throughput in 8 bit was 14 Gbit/s. Liu Zhi et al [6] studied effective carrier recovery for high-order QAM and classical phase detector driven decision. They proposed an algorithm that uses a phase detector and a coaxial cable and AWGN channel for a transmission channel. Experiments were conducted with 8 bits and gave a 960 KHz frequency (AWGN channel) and 690 KHz (coaxial cable) by a transmission throughput of 6.9 Mbit/s.

The rest of this paper is organized as follows: Section 2 describes the developed system. Section 3 shows the obtained results, provides the details of experiments and some discussions. Section 4 gives the main conclusion.

2. METHODOLOGY

In this section, we will show the three steps followed to develop the digital modulator. The first is based on a pipeline CORDIC processor on eight stages in serried and the second is based on a pipeline processor single stage and the third based on a pipeline CORDIC without phase accumulator. In comparing the three architectures, we focus on the CORDIC algorithm has a sine wave generator base [7]. The essential element is used to obtain maximum sampling frequency and better throughput.

2.1. The QAM digital modulation (Fig. 1)

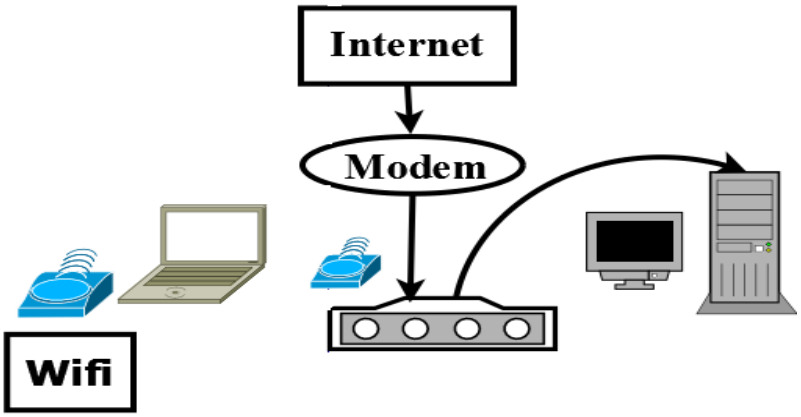


Figure 1. Experiment environment and used digital modulator.

The digital modulator (QAM) is most necessary step in data communication between the transmitter and the receiver. It combines amplitude and phase modulation concurrently on the same carrier to dual the transmission rate. Every point is exhibited by Equation 1:

$$S(t) = A\cos(wt) + B\sin(wt) \quad (1)$$

Where W, is the angular frequency in rad (s^{-1}), A and B are the coordinates on the axes I and Q. The amplitude and the phase of this signal calculated by equation 2:

$$S = \sqrt{A^2 + B^2}\cos\left(wt + \arctan\left(\frac{B}{A}\right)\right) \quad (2)$$

Amplitude modulations are all points on I axes and the phase modulations are all points on the circle. QAM is used in several areas such as audiovisual for information and components transfer in color television (PAL and NTSC) [8]. This element is a high-speed modulator sending an electrical signal to power amplifier which shows parameters working in real time, and also a channel encoding circuit to compensate the noise on the transmission channel [9]. The internet modem illustrated in figure 1 is used to generate and facilitate communication between people (call, SMS... etc.) [10].

2.2. The architecture of a modulator

The digital modulator (QAM) consists of three elements operating in digital mode "the encoder, the phase accumulator and wave generator" (Fig. 2).

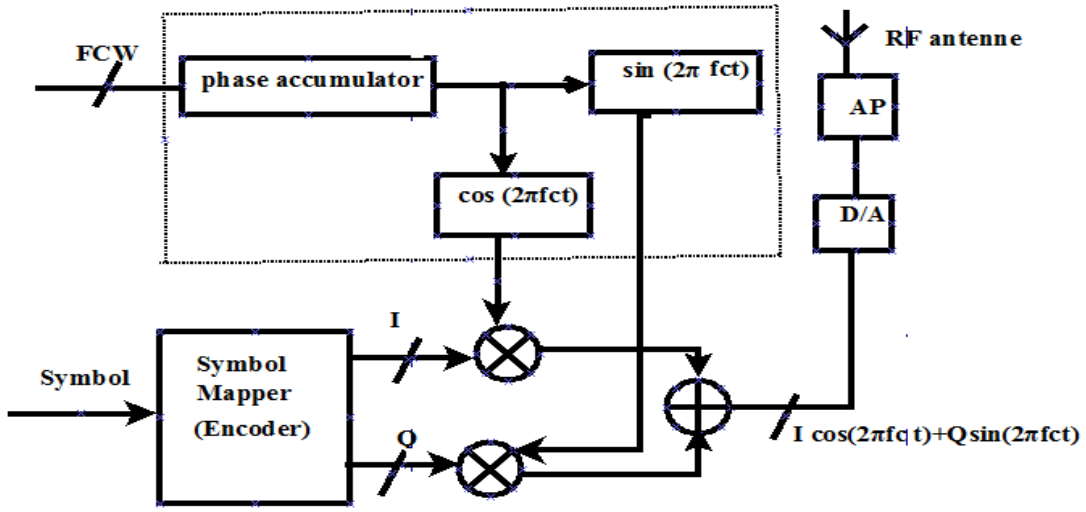


Figure 2. Digital modulator Architecture

More details regarding these devices are detailed in the following sections.

2.2.1 The Encoder

The first step is to bring the needed information to exchange a set of binary information using coding techniques. This is done by an encoder consisting of a small address size memory which converts the series of M-bit symbol component to make them compatible with a selected modulation type. For example in phase modulation, a series of M-bits will be replaced by the corresponding phase of digital wave signal to produce modulator output. The objective of this component is to convert the binary data into radio frequency signals and facilitate their transfer from one part to another as shown in figure 3.

Figure 3. Encoders architecture

2.2.2. The Phase accumulator

The second step of generating a digital modulator (QAM) is the choice of the phase accumulator. It is necessary to generate phase values (theta) in order to have the output as a digital wave signal. Its architecture is shown in figure 4.

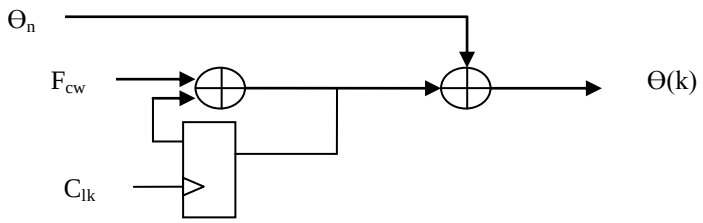


Figure 4. Phase accumulators architecture

The effective frequency "f" of the resulting modulated signal is expressed by the following equation:

$$f = \frac{f_{clk} \times F_{cw}}{2\pi} \quad (3)$$

f_{clk}: clock frequency
F_{CW}: Word control the frequency corresponding to the phase increment applied to each system clock period
Θ_n: a phase shift when the considered modulation uses this parameter to transmit information
The k^{th} phase word produced by this stage is:

$$\theta(k) = k \times F_{cw} + \theta_n \quad (4)$$

Its function is to generate the phase term which corresponds to the instantaneous phase of the sample sinusoid produced by the modulator.

2.2.3. Digital wave generator

The most important study of these elements is the digital wave generator where various techniques are used. The best architecture will allow obtaining a faster modulator amplitude and phase and also more efficient architecture. Figure 5 shows the output of the phase accumulator which is connected to the most critical portion of the digital modulation architecture "the digital wave generator" which must calculate the cosine of the phase term produced by the accumulator stage [11]. Usually, the sine wave generator does not generate a signal, it gives a value based on the input value “theta” which gives as output “cos (theta)” or “sin (theta)”.

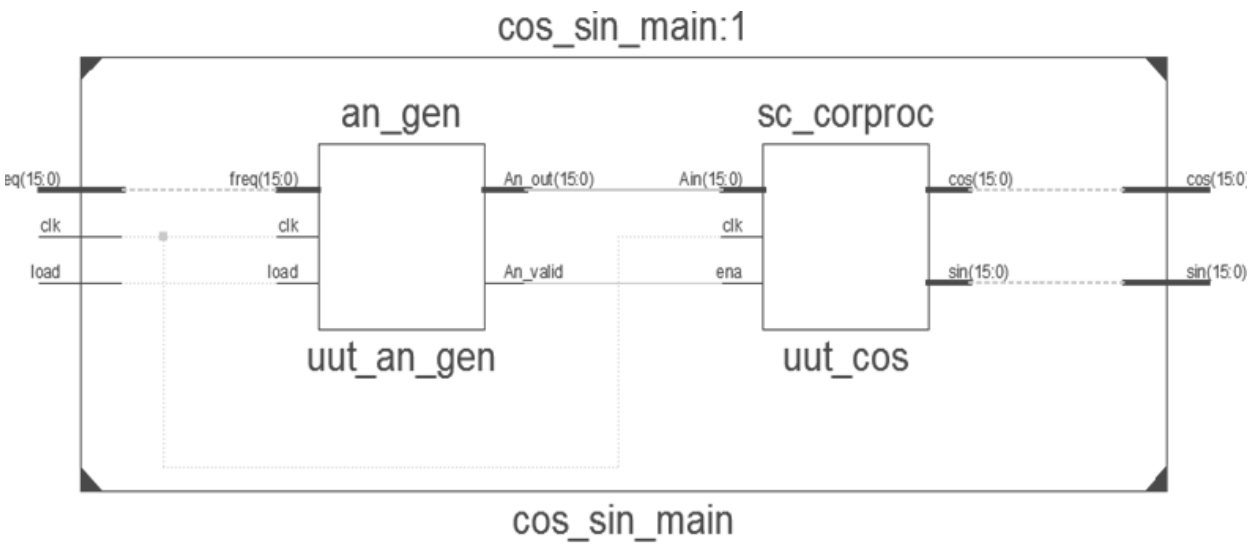


Figure 5. Sinusoids generator architecture

2.3. QAM digital modulation principles

The modulation is a very important step to transmit the signal. We focus on the sine wave generator illustrated on figure 5. A simple algorithm is employed to calculate the speed of which is the coordinate numerical calculation by rotation (CORDIC). There are three technologies presented in this work. The first pipeline CORDIC 8 stages, the second pipeline CORDIC and the third pipeline CORDIC without phase accumulator. These three architectures are explained in the following sections [12], [13].

2.3.1. Cordic algorithm principle

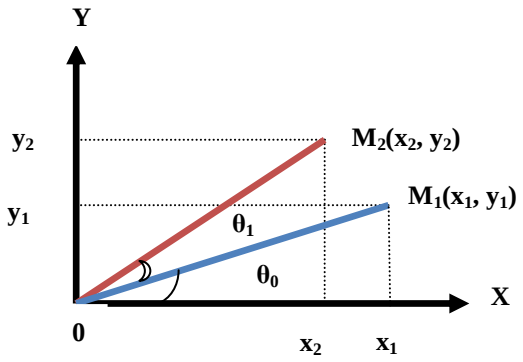


Figure 6. Decomposition of angle θ in several micro-rotations

Indeed, for a value of Θ taken in the interval]-$\frac{\pi}{2}$;$\frac{\pi}{2}$[. Volder has shown that there is a sequence of d_i values with $d_i \in \{-1, 1\}$ for which:

$$\theta = \sum_{i=0}^{\infty} d_i \arctan 2^{-i} \quad (6)$$

So make a Θ rotation angle can be written in the following matrix form:

$$\overrightarrow{v'} = \prod_{i=0}^{\infty} \cos\left(d_i \cdot \arctan 2^{-i}\right) \cdot \prod_{i=0}^{\infty} \begin{pmatrix} 1 & \cos\left(d_i \cdot 2^{-i}\right) \\ d_i.2^{-i} & 1 \end{pmatrix} \cdot \vec{v} \quad (7)$$

2.3.2. CORDIC algorithm architecture

For fast computation of sine generators various parameters, the samples CORDIC algorithm is used. There are three architectures: a single stage pipelines CORDIC operator and eight stages in serried and pipeline CORDIC without phase accumulator to generate various modulation (QAM_1 QAM_2 QAM_3) .The comparative studies conducted between the architectures showed in table 1 illustrate these differences by comparing several relevant parameters of each architecture[15].

Table1. Comparison of Several Relevant Parameters of Various Cordic Algorithms

Pipeline CORDIC (a single stage , eight stages)	Pipeline CORDIC without phase accumulator
High cells occupancy	Low cells occupancy
Minimum frequency	Maximum frequency
n stage for (n-1) number of bit	n stage for (n-1) number of bit removed the stage of phase accumulator
(n + 1) adder subtracted for each of the three path computing (X, Y and Z)	(n + 1) full adder subtracted for each of the three calculation axes (X, Y, Z)

3. RESULTS AND DISCUSSIONS

As mentioned earlier the three techniques were implemented on FPGA destination type Xilinx virtex5-XC5LX110T and the maximum frequency announced for the manufacturer of this type of circuit is 550 MHz. the ISE 12.2 software as well as VHDL are used. The three settings frequency, cells, and throughput are as follows:

$$\begin{cases} \text{frequency}_{QAM3} > \text{frequency}_{QAM2} > \text{frequency}_{QAM2} \\ \text{cells}_{QAM3} < \text{cells}_{QAM2} < \text{cells}_{QAM1} \\ \text{throughput}_{QAM3} > \text{throughput}_{QAM2} > \text{throughput}_{QAM1} \end{cases} \quad (8)$$

3.1. Implementation of CORDIC algorithm

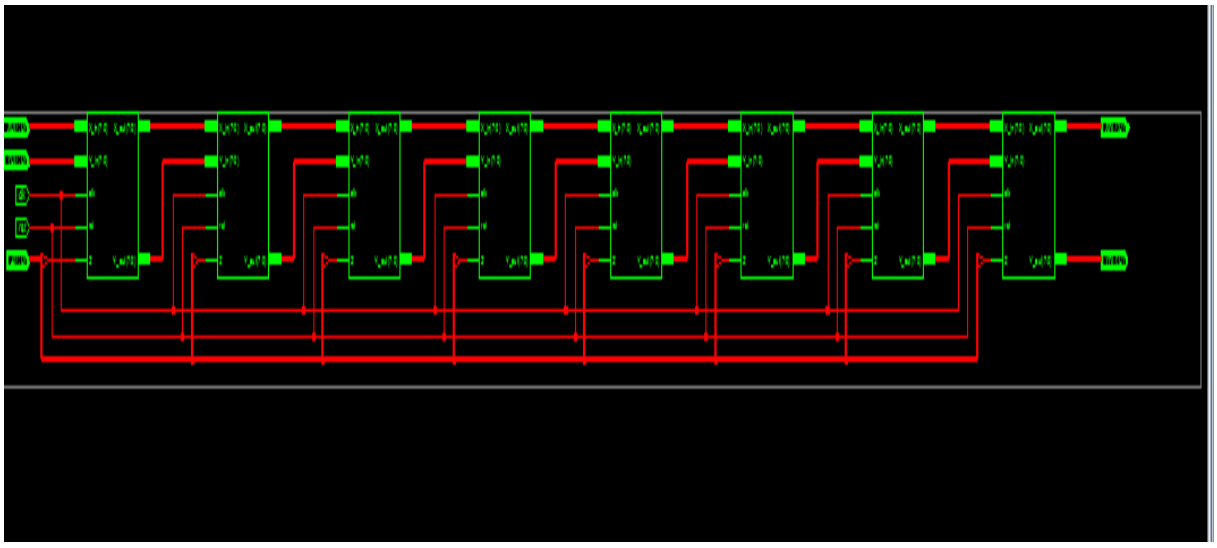


Figure 7. The implementation of a pipelined CORDIC eight (8) stages on the FPGA

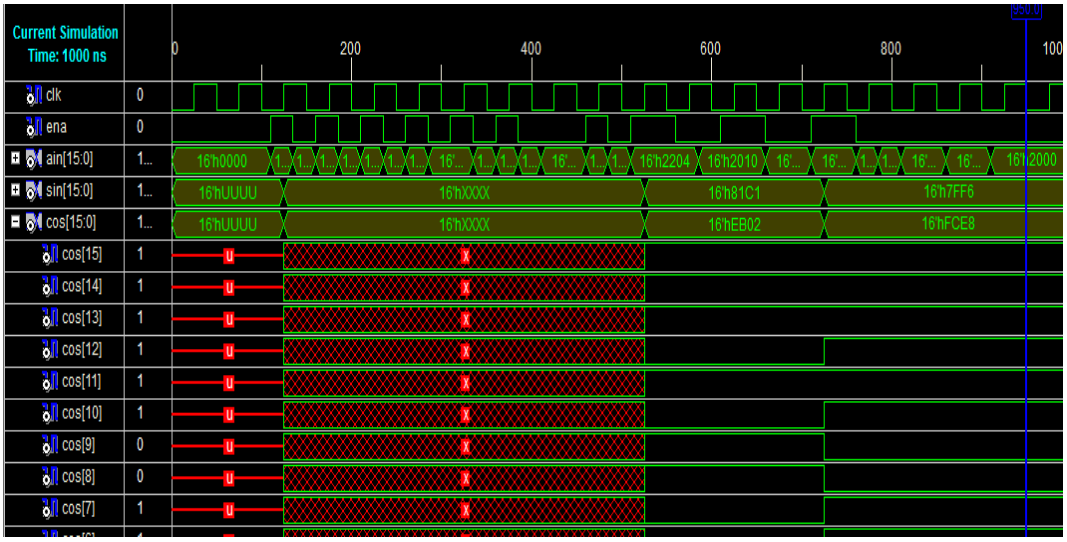


Figure 8. Simulation results of pipeline CORDIC 8 stages

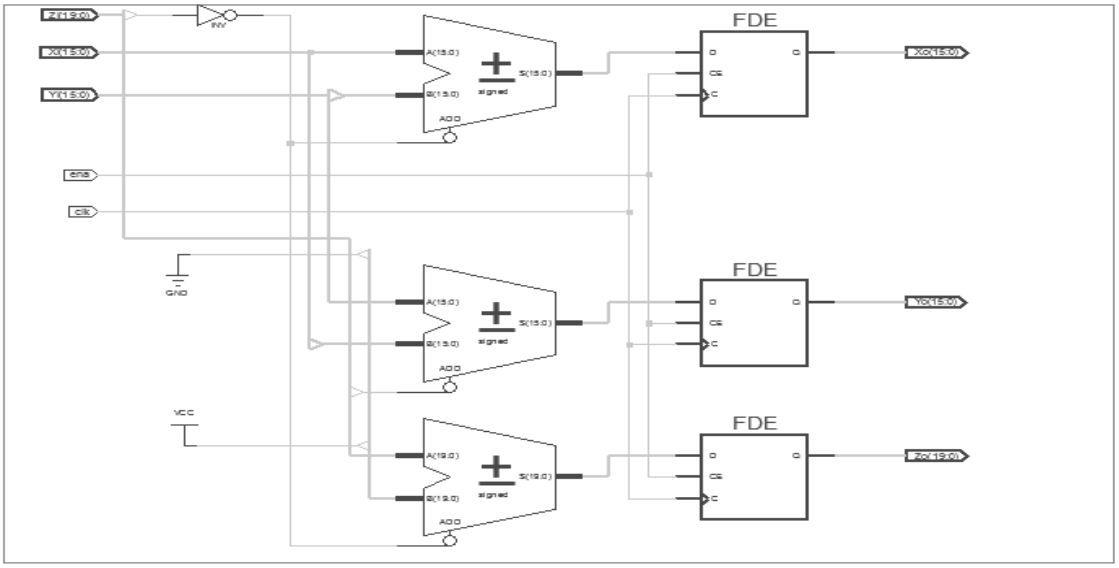


Figure 9. The implementation of a pipelined CORDIC 1 stage

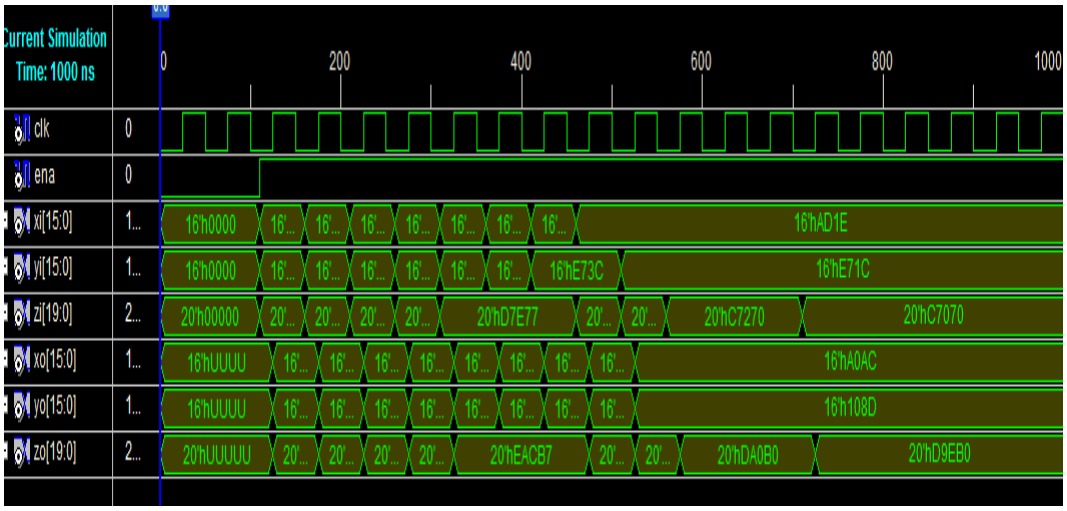


Figure 10. Simulation results of pipeline CORDIC algorithm in one stage

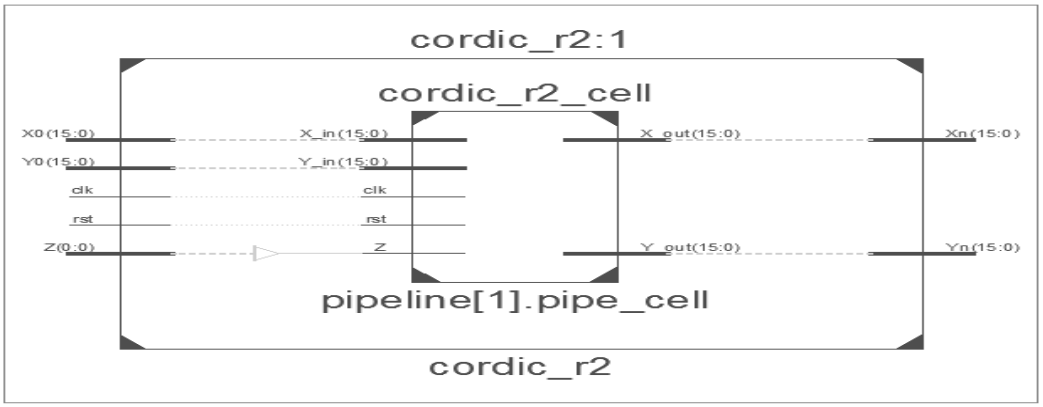


Figure 11. The implementation of a pipeline CORDIC without phase accumulator complete digital QAM_1 modulator

CORDIC algorithm has been originally designed as a tool for numerical calculation. This work is particularly interested on the installation of eight stages pipelined CORDIC architectures as illustrated in Figure 7 and figure8, and pipeline CORDIC 1 stage shown in figure 9 and figure10. The proposed architecture is the pipeline CORDIC without phase accumulator as presented in figure 11, specialized digital signal processing as explained in table 2 and to simplify (Figures 7 and 8). The three architectures are located on the field programmable gate array (FPGA) Virtex-5 XC5LX110T kind of Xilinx that are part of the family of programmable electronic components. Also, using the ISE 12.2 software, this is a description of software simulation and programming of digital circuits and systems on programmable components, with as a Very High Speed Integrated Circuit Hardware Description Language (VHDL) to represent the behavior and the architecture of a digital electronic system.

In this chronogram, the phase cosine and sine are available after 8 cycles of clocks. The architectures proposed in this study are the implementation of both digital modulators QAM with pipeline CORDIC algorithm with 1 stage and 8 stages (Fig. 12).

There are various architectures based on a CORDIC processor: the first architecture is based on a pipeline CORDIC eight stages in serried. It is used in the sinusoid generator computing for the slow modulator, but takes several cells in the FPGA circuit (Figure 12).

In Table 2, the results of the implementation of the digital modulator (QAM_1) are presented. From this table, it can be observed that the number of cells is higher for 16 bits. This parameter disturbs the transmission period of the modulated signal. The occupation of the logic block is raised to 467 cells. The transmission of this signal takes a long time and therefore a minimum throughput. So, we conclude that this modulator is slow.

3.2. Complete digital QAM_2 modulator

The second architecture is based on pipeline CORDIC processor. It is used in the sinusoid generator computing for medium modulator, but takes several cells in the FPGA circuit Figure 12. In table 2, the results of the digital modulator (QAM_2) based on a pipeline CORDIC are shown. This method is the same as that of QAM_1 modulator, but the principle of this algorithm is in the pipeline processor based on sine wave generator removing the seven cells of the pipeline CORDIC. This member reduces the space in the digital circuit. The frequency is higher than QAM_1 frequency and is exhibited optimal throughput on different bits. It can be concluded that this modulator is faster than the first modulator.

3.3. Complete digital QAM_3 modulator

The third architecture is based on a pipeline CORDIC processor without phase accumulator. It is used in the fast sinusoid generator computing, but takes medium cells in the digital circuit FPGA figure 12. Table 2, shows the results of the proposed architecture. It is the modulator based on a pipeline CORDIC without phase accumulator. The QAM_3 is the same method as that of QAM_2 modulator, but the principle of this algorithm is in the pipeline processor based sine wave generator removing the cells of the phase accumulator. This member reduces the space in the digital circuit. The frequency is higher than the clock frequency of the FPGA and is exhibited optimal throughput on different bits. It can be concluded that this modulator is faster than QAM_1 and QAM_2.

3.4. Comparison between QAM_1, QAM_2 and QAM_3

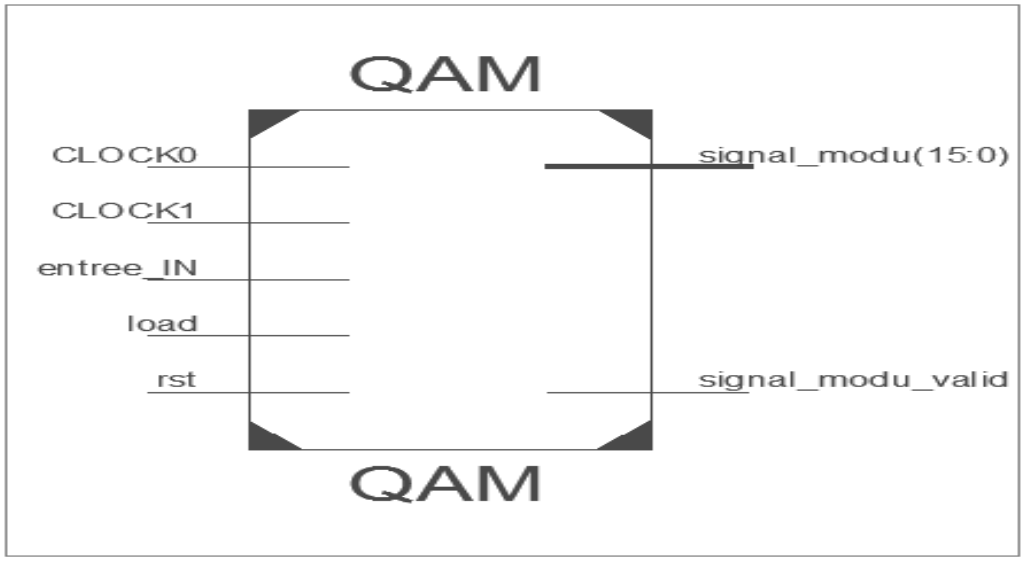
Table 2, shows the implementation of the digital modulator based on CORDIC algorithms

Table 2. Results of various Qam Digital Modulator

n (16bits)	The maximum frequency (MHz)	LUT slice (19200)	LUT slice register (19200)	Power (m watt)
QAM_1	232.52	467	384	267.18
QAM_2	237.102	102	51	266.84
QAM_3(proposed architecture)	284.511	92	51	266.84

In this study it is required to determine the architecture that generates the large sampling frequency. First, we use the implantation of a sinusoidal generator based on a pipeline CORDIC 8 clock cycles produced a sample, this performance decreases the sampling frequency and the bit rate. In the second study a 1 stage of CORDIC pipeline is used, the sampling frequency of this algorithm is equal to the clock frequency (FPGA circuit) in various bits because a single cycle uses to obtain a sample ($f_{samples}=f_{clk}$). Then, in the third study a pipeline CORDIC without phase accumulator is employed, the sampling frequency is higher than the clock frequency. The implementations for various architectures are presented in figure 12.

From these results, it can be deducted that the architecture proposed in a pipeline stage without phase accumulator processes low power consumption, this is due to the removed numbers of the pipeline stages, which decrease the operating frequency compared to eight stages in 16 bits. Figure 13 shows the simulation results of the proposed digital modulator. The chronogram below illustrates this validated architecture, the signal of $CLOCK_0$, the operation of this modulator is stopped directly.



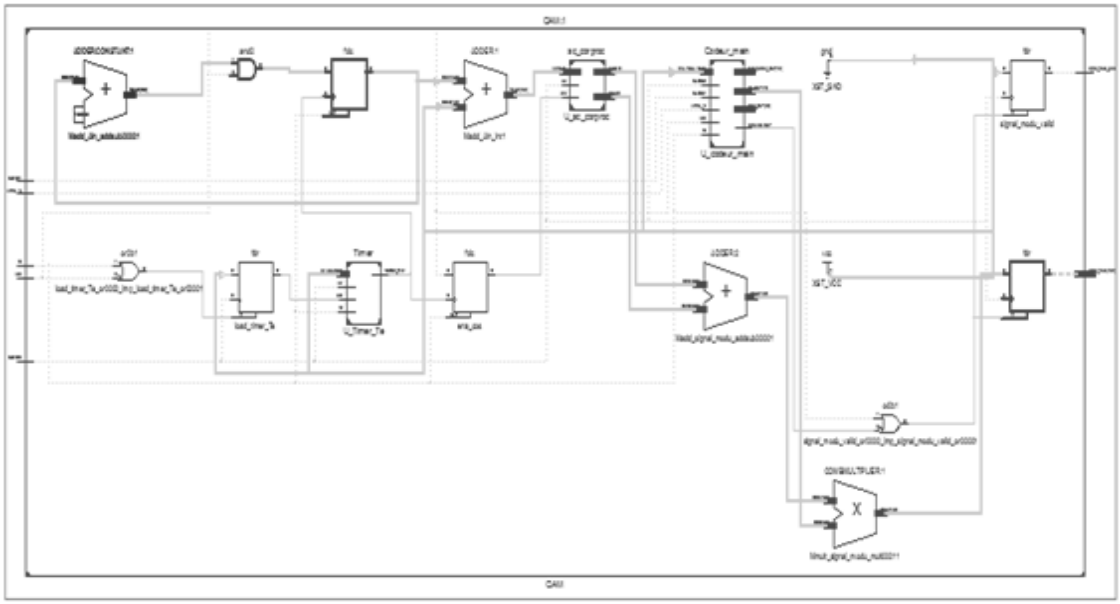


Figure 12. RTL diagrams of digital QAM modulator with CORDIC operator

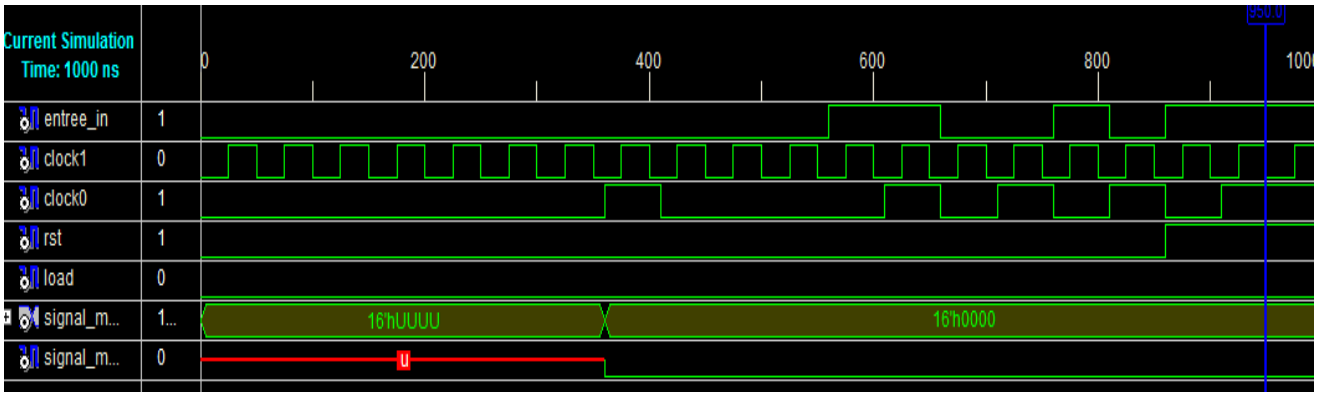


Figure 13. Simulation results of digital modulator on amplitude and phase with pipeline CORDIC

4. CONCLUSION AND PERSPECTIVES

In this work, several methods dedicated to the optimization of high-speed data transmission in the telecommunications system are presented. A comparative study was established between two CORDIC-based algorithms with a sinusoidal generator. The best results were obtained in the QAM modulator, with a CORDIC single cell operator pipeline that generates a frequency of 284.511MHz and uses a minimum number of cells (92). Therefore, these performances increase the speed and efficiency of this modulator.

In the future work, it will be interesting to extend the present study on digital demodulation based on a linear feedback shift register (LFSR) established on the same type of circuit. The task this circuit is the reception of the signal emitted by the modulator to analyze both functions at the same time and to apply the two functions in the field of advanced telecommunications.

5. ACKNOWLEDGEMENTS

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REFERENCES

[1] Yamada E., Kikuchi N., Sano A., Kobayashi T., Shibata Y., Ishii H. & Miyamoto Y., 2012. 86 Gbit/s Pdm 16-qam signal transmission using inp optical iq modulator, *Electronics Letters*, Vol . 48 (23), 1486 – 1487.

[2]Paulsson K., Hübner M. &2008. Cost-and power optimized FPGA based system integration: methodologies and integration of a low-power capacity-based measurement application on Xilinx FPGAs, Proceedings of Design, automation and test'2008, Europe, 50-55.
[3]Arnould G., 2006. Etude et conception d'architectures haut-débit pour la modulation et la démodulation numériques, Manuscript of thesis, LICM, University of Metz, 142 p.
[4] Xilinx. ISE 12.2i software manuals. Xilinx; 2008.
[5]Winzer P. J., Gnauck A. H., Doerr C. R., Magarini M. & Buhl L. L., 2010. Spectrally efficient long-haul optical networking using 112-gb/s polarization-multiplexed 16-qam, *Journal of Lightwave Technology* Vol . 28 (4), 547 - 556.
[6]Zhi L., Zhou ., Qing L. & Xiaoyang Z., 2007. Efficient carrier recovery for high-order qam, Proceedings of Consumer Electronics'2007, Las vegas, Nv, Usa,1-2.
[7] Liu Y. , Fan L. & Ma T., 2014. A modified cordic fpga implementation for wave generation , *Circuits, Systems, and Signal Processing*, Vol . 33 (1), 321–329.
[8] Kurakake T., Nakamura. & Oyamada K., 2004.A blind 1024-qam demodulator for cable television, Proceedings of International Zurich Seminar on Communications'2004, Zurich, Switzerland, Switzerland, 136 – 139.
[9] Trung H. D, Tuan D. T. & Pham A. T., 2014. Pointing error effects on performance of free-space optical communication systems using sc-qam signals over atmospheric turbulence channels, International Journal of Electronics and Communications, Vol . 68 (9), 869-876.
[10] Mohini., Priya ., Sur S.N., Bera S., 2019. labview-based software and hardware implementation of 16-qam modem, Proceedings of Advances in Communication, Devices and Networking'2019, Singapore, 221-227
[11] Naik R. & Nadaf, R., 2015. Sine-cosine computation using cordic algorithm, International Journal of Advanced Research in Computer and Communication Engineering, Vol . 4, (9), 44-48.
[12] Boudjema S. &Saouchi K., 2015. The optimal implementation of a generator of sinusoid, *American Journal of Applied Sciences*, Vol . 12 (8), 593-600.
[13] Kavya S., Uma B.V. &Sagar D.M., 2014. Calculation of sine and cosine of an angle using the cordic algorithm, *International Journal of Innovative Technology and Research*, Vol . 2 (2), 891 – 895.
[14] Xu R., Jiang Z., Huang H. & Dong C., 2015. An optimization of cordic algorithm and fpga implementation, *International Journal of Hybrid Information Technology*, Vol . 8 (6), 217-228.
[15] Kang C. Y. & Swartzlander E.E., 2006. Digit-pipelined direct digital frequency synthesis based on differential cordic, *Ieee Transactions on Circuits and Systems I*, Vol . 53 (5), 1035-1044.